Ruslan Bukin

William Gates Building, 15 JJ Thomson Ave,
Cambridge, CB3 0FD, UK
+447522084566
br@bsdpad.com

Professional Experience

Since Sep 2014 Senior Research Software Engineer **Computer Laboratory, University of Cambridge, UK**

description CHERI team

- Developed **RISC-V ISA** support for FreeBSD's native **bhyve hypervisor**. (review stage)
- Developed the new **Hardware Tracing Framework (HWT)** for FreeBSD (review stage)

- Added base FreeBSD support for the **ARM Morello Board** – the joint project ARM/Cambridge. I wrote Panfrost GPU kernel driver for the ARM Mali Midgard/Bifrost GPUs. I wrote Mali D32 Display Processors drivers and ARM Komeda DRM parts. I wrote the Cadence I2C controller driver.
- Added FreeBSD base support for **ARM Neoverse N1** – a new server-class architecture (a Cortex successor) from ARM Ltd. I've developed PCI-e driver; Developed support for ARM System MMU v3.2 and formed **generic IOMMU framework** in the FreeBSD. This is about 1 year of work.
- I ported the **FreeBSD Operating System** to the **RISC-V** Instruction Set Architecture (ISA) designed by University of California, Berkeley. From zero to a complete working system. The port includes kernel debugger support, SMP multiprocessing, DTrace support, a set of device drivers. The port covers support for FPGA implementations (RocketChip), simulators and emulators (Spike, QEMU) and the real hardware (HiFive Unleashed board).
- I added support for **Intel Software Guard Extensions (SGX)** to FreeBSD. Intel SGX allows to manage isolated compartments "Enclaves" in user VA space. I wrote the SGX kernel driver and ported Intel Linux SGX SDK to FreeBSD. The SGX driver includes an optional linux ioctl compatibility layer.
- Added FreeBSD OS support to U.S. Government Furnished Equipment (GFE) RISC-V cores synthesized on an FPGA; developed device drivers for Xilinx Ethernet controller, Xilinx DMA engine.
- Brought up FreeBSD OS support to Intel Stratix 10, Intel Arria 10, Intel Cyclone V FPGA/ARM SoCs, including support for programming FPGA.
- Developed Device-model (DM) project. DM allows to emulate different SoC peripherals in software. It runs bare-metally on a secondary core of a SoC, providing peripherals to the main core. I ported the PCI stack of BHyVe hypervisor including BHyVe Intel e1000 ethernet device to DM.
- I developed xDMA framework. xDMA is a DMA abstraction layer that standardize the interface between DMA engine drivers and peripheral device drivers. I wrote the framework and added support (kernel drivers) for a few DMA engines found in various ARM and MIPS CPUs including ARM PL330, Altera Module Scatter-Gather DMA Engine (mSGDMA), Ingenic PDMA controller.
- Developed support for Intel Processor Trace and ARM Coresight hardware tracing technologies to FreeBSD. I wrote the kernel part using existed Hardware Perfomance Monitoring Counters (HWPMC) framework and developed pmctrace userspace application. This is currently on review.
- I added support for ARMv7,v8 and CHERI CPUs to HWPMC framework.
- I added support for ARMv8, RISC-V to DTrace comprehensive dynamic tracing framework.
- I brought up support for some ARM and RISC-V system-on-chips including Altera SOCFPGA, Qualcomm MSM8916, lowRISC SoC covering minimal support required.

▪ I wrote various device drivers for FreeBSD including Virtio MMIO bus, Synopsys DesignWare MMC controller, Synopsys DesignWare 3504-0 Universal 10/100/1000 Ethernet MAC, Generic ARM PCI controller, Cadence Quad SPI Flash controller, ARM Generic Timer, Xilinx AXI Quad SPI controller.
▪ I developed Virtio networking for CHERI CPU, Virtio block device frontends for a heterogeneous communication between different in kind CPU cores of Altera SOCFPGA: ARMv7 32-bit little-endian and CHERI 64-bit big-endian core synthesized on the FPGA.

Since May 2022 — Engineer **Capabilities Limited** (part time)
▪ Implemented memory-safety for userspace drivers and rendering: memory-safe kernel DRM, memory-safe kernel Panfrost GPU drivers, memory-safe Wayland window server, memory-safe KDE, memory-safe mesa3d
▪ Added CHERI support to ARM Trusted-Firmware (TF-A). This includes BL2, BL31 bootloaders (BL1 is running in SRAM – no cheri tag controller – skipped)
▪ Attempt to add CHERI support to industry-standard UEFI (TianoCore EDKII), 30% done, stalled due to weak pointer provenance in UEFI

Technical Skills

Languages	C, Assembly, BSD/GNU Make, Python, Shell
Technologies	Intel SGX, Intel PT, ARM Coresight, ARM TrustZone, ARM TF-A, ARM SCMI, ARM PSCI, ARM System MMU.
Instruction Sets	RISC-V, MIPS, ARMv7/v8
Operating Systems	FreeBSD, MDEPX RTOS
CAD	Cadence Orcad/Allegro, Solidworks

Links

https://github.com/machdep/mdepx
https://github.com/freebsd/freebsd
https://github.com/CTSRD-CHERI/device-model-riscv

Publications

Panfrost Kernel Driver	https://freebsdfoundation.org/wp-content/uploads/2021/08/The-Panfrost-Driver.pdf
Defending DMA with CHERI Capabilities	https://dl.acm.org/doi/pdf/10.1145/3458903.3458910

Education

2002 – 2008 — **BSc, Computer Science**,
Peoples' Friendship University of Russia, Moscow, Russia.

Personal

Nationality	**Russian, British**.
Marital status	**Single**.

Languages

First Language	**Russian**
Fluent	**English**